CLAIMS

What is claimed is:

1. A system comprising:

a plurality of programmable logic devices, including at least a first and a second programmable logic device, the first and second programmable logic devices coupled to receive programmable logic device configuration code from a first and a second EEPROM associated therewith;

a first serial bus coupling the first EEPROM with a common configuration logic, and a second serial bus coupling the second EEPROM with the common configuration logic;

a processor coupled to the common configuration logic, wherein the processor is also coupled to a memory subsystem;

wherein the processor is capable of transferring programmable logic configuration code from its memory subsystem into the first EEPROM.

2. The system of Claim 1, wherein the first & second EEPROM are located on separate PC boards of the system.

3. The system of Claim 2, wherein the first and second serial busses are JTAG busses.

4. The system of Claim 2, wherein the processor is coupled to the common configuration logic through a third serial bus.

5. The system of Claim 4, wherein the third serial bus is a serial bus of the IIC type.

6. The system of Claim 4, wherein the programmable logic devices are field programmable gate arrays.

7. The system of Claim 6, wherein at least one EEPROM is located on the same integrated circuit as a field programmable gate array.

8. The system of Claim 6, wherein the common configuration logic is embodied in a field programmable gate array.9. The system of Claim 6, wherein the common configuration logic is embodied in a field programmable gate array coupled to receive configuration code from an EEPROM, the EEPROM coupled to be programmable by the processor through the common configuration logic.

10. The system of Claim 6, further comprising

network interconnect, for coupling the system to a network; and

wherein a processor of the system is capable of transferring configuration code from a configuration code database on a network server through the common configuration logic and writing the configuration code into an EEPROM of the system.

11. The system of Claim 10 wherein at least one of the programmable logic devices performs system management functions and couples to a system management bus.

12. The system of Claim 10 wherein the processor is coupled to the common configuration logic through a system management processor, the system management processor being coupled to the common configuration logic through the third serial bus.

13. The system of Claim 10, wherein at least one of the programmable logic devices is configured to serve as the common configuration logic.

14. A method of in-system programming of EEPROMs, the EEPROMS being coupled to provide configuration code to FPGAs, comprising:

transferring at least portions of a configuration code file to a system management processor of the system;

providing a system management bus coupling the system management processor to common configuration logic, the common configuration logic coupled to a plurality of serial busses coupled to a plurality of the EEPROMS;

setting selection logic to designate an active serial bus coupled to an EEPROM to be programmed;

verifying compatibility of the configuration code file with the active serial bus;

erasing at least a portion of the EEPROM to be programmed;

writing at least a portion of the configuration code file from the system management processor, over the system management bus, over the active serial bus, and into the EEPROM; and

causing configuration code to be loaded from the EEPROM into at least one FPGA.

15. The method of Claim 14, wherein the configuration code is located on a drive of the system.

16. The method of Claim 14, further comprising the steps of locating the configuration code file on a server of a network, and downloading the configuration code file to the system.

17. The method of Claim 16, wherein the step of causing configuration code to be loaded from the EEPROM into at least one FPGA is performed without cycling power.

18. A method of self-repairing a system by in-system programming of EEPROMs, the EEPROMS being coupled to provide configuration code to FPGAs, comprising:

detecting an error in FPGA configuration code as the FPGA configuration code is fetched from an EEPROM;

locating an FPGA configuration code file in a database;

transferring at least portions of the configuration code file to a system management processor of the system;

providing a system management bus coupling the system management processor to common configuration logic, the common configuration logic being coupled to a plurality of serial busses coupled to a plurality of the EEPROMS;

setting selection logic to designate an active serial bus coupled to an EEPROM to be programmed;

verifying compatibility of the configuration code file with the active serial bus;

erasing at least a portion of the EEPROM to be programmed;

writing at least a portion of the configuration code file from the system management processor, over the system management bus, over the active serial bus, and into the EEPROM; and

causing configuration code to be loaded from the EEPROM into at least one FPGA.